CLAIMS

What is claimed is:

1. A method for processing bundled instructions through execution units of a processor, comprising the steps of:

fetching a first bundle of singly-threaded instructions;

distributing the first bundle to a first cluster of the execution units for execution therethrough;

fetching a second bundle of singly-threaded instructions; and

distributing the second bundle to a second cluster of the execution units for execution therethrough.

2. A method of claim 1, further comprising processing the first bundle within the first cluster.

3. A method of claim 1, further comprising processing the second bundle within the second cluster.

4. A method of claim 1, further comprising the step of architecting data from the first cluster to a first register file.

5. A method of claim 4, further comprising the step of committing architected state from the second cluster to the first register file.

6. A method of claim 4, further comprising the step of architecting data from the second cluster to a second register file.

7. A method of claim 1, the step of fetching the first bundle comprising decoding instructions into the first bundle of the singly-threaded instructions.

8. A method of claim 1, the step of fetching the second bundle comprising decoding instructions into the second bundle of the singly-threaded instructions.

9. A method of claim 1, further comprising the steps of:

fetching a third bundle of singly-threaded instructions;

distributing the third bundle to the first and second clusters of the execution units for execution therethrough; and

bypassing data between the clusters, as needed, to facilitate processing of the third bundle through the clusters.

10. A method of claim 9, the step of bypassing utilizing a latch to couple the data between the clusters.

11. A method of claim 9, further comprising the step of selecting a configuration bit prior to the steps of fetching the third bundle, distributing the third bundle, and bypassing.

12. A method for processing bundled instructions through execution units of a processor, comprising the steps of:

fetching a first bundle of singly-threaded instructions;

distributing the first bundle to two or more clusters of the execution units for execution therethrough; and

bypassing data between the clusters, as needed, to facilitate processing of the first bundle through the clusters.

13. A method of claim 12, further comprising the steps of.

fetching a second bundle of singly-threaded instructions;

distributing the second bundle to one of the clusters for execution therethrough;

fetching a third bundle of singly-threaded instructions; and

distributing the third bundle to another one of the clusters units for execution therethrough.

14. A method of claim 13, further comprising the step of selecting a configuration bit prior to the steps of fetching the second bundle, distributing the second bundle, fetching a third bundle and distributing the third bundle.

15. In a processor architecture of the type having two or more clusters of execution units for processing instructions, the improvement comprising:

a thread decoder for grouping instructions into singly threaded bundles and for distributing the bundles to the clusters according to either a wide mode or throughput mode of operation.

16. In a processor architecture of claim 15, the further improvement wherein each cluster comprises a core and register file.

17. In a processor architecture of claim 15, the further improvement wherein the thread decoder distributes bundles of singly-threaded instructions through a multiple clusters in the wide mode of operation, and wherein the thread decoder distributes bundles of singly-threaded instructions through one of the clusters in the wide mode of operation.